Modeling Millimeter-Wave IC Behavior for Flipped-Chip Mounting Schemes

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***Abstract*— A circuit topology is presented for modeling flipped-chip-mounted monolithic microwave integrated circuits (MMIC's) at microwave frequencies. The proposed topology especially models the loss of isolation due to the flipped-chip structure. Both coplanar and microstrip flipped chips are circuit modeled and their results compared to full numerical simulations and to scale-model measurements. Both measurements and numerical modeling show resonances in the millimeter-wave range.**

***Index Terms*—Flip chip, microwave packaging, MMIC packaging.**

I. Introduction

IN RECENT years there has been an intense effort to reduce the cost of manufacturing microwave integrated systems. Toward that end, packaging schemes such as chip-on-board, chip scale packaging, and flipped chip have received great attention. These schemes have the advantages of greatly reduced size and weight, compatibility with automated manufacturing, and improved electrical performance. They especially find use in multichip assemblies where several chips are mounted on a single (motherboard) substrate.

The subject of this paper is microwave-circuit modeling of flip-chip mounted monolithic microwave integrated circuits (MMIC's). Flipped-chip mounting has the advantage of a short, reproducible, electrical connection to a printed circuit board. Wire bonds are eliminated. Flip-chip technology has been used extensively by IBM [1] for mounting microprocessors and, more recently, by Hughes [2], [3] for X- and Ku-band MMIC's. The microwave characteristics of the transition from motherboard to chip has been simulated [4] and a circuit model derived [5], but only for a single transition. The work reported in this paper is concerned with the more global behavior of the flipped "package," particularly the proper modeling of input–output isolation. Poor isolation clearly limits the performance of mixers, switches, and gain blocks. Modeling isolation requires consideration of the electromagnetic behavior of the overall package. In the case of flipped chips, this means consideration of bump ground location and number, the size of the chip, the characteristics of the underfill, and the characteristics of the motherboard.

In particular, we will consider flipped MMIC's of both coplanar and microstrip types. Coplanar MMIC's are far more commonly flip mounted than microstrip since coplanar MMIC's have all grounds immediately available on one surface. Also, coplanar circuitry requires no backside processing and allows the use of a thicker, more physically robust chip. On the other hand, many MMIC manufacturers have a considerable investment in microstrip design tools and may wish to make full use of their investment by flipping microstrip circuits. Thus, we will compare the two in terms of isolation.

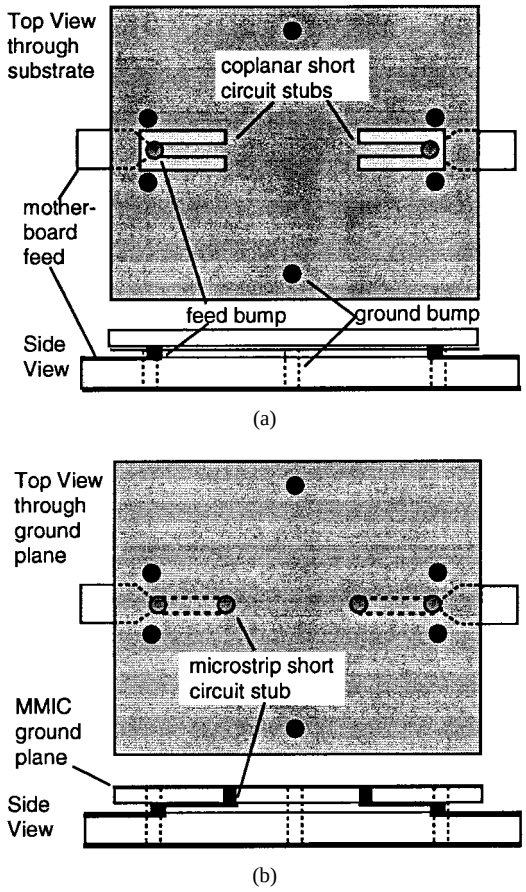

Fig. 1. Side and top view of (a) coplanar and (b) microstrip flipped MMIC's consisting of two short-circuit stubs and six bump grounds.

Fig. 1 shows illustrations of the two canonical structures we are considering. A motherboard (of glass for example) has microstrip feeds on it which inject current through a bump into the circuitry on the surface of the flipped chip. In the illustration, the flip-chip test circuits consist of coplanar and microstrip short-circuit stubs connected to the input and output bumps of each chip. For the microstrip case, the chip ground is at the very top of the structure, while the semiconductor

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substrate is at the top in the coplanar case. In both cases, the chip ground is connected to the motherboard ground by bumps on the chip surface and vias through the motherboard (the six black circles in the two cases illustrated). Ideally, the structures shown in the figure should have infinite isolation between the motherboard input and output ports. However, the inductance of the bump/via connection between the flipped ground plane and the motherboard ground plane causes the isolation to deteriorate.

In the next section, we present a circuit model for the flipped-chip package. In Section III, measurements of a scale model are described and compared to the results from the circuit model. The measurements and modeling bring up basic issues, which are discussed in Section IV. Conclusions are presented and discussed in Section V.

II. Circuit Model of a Flipped Chip

The goals of circuit modeling complex structures are to: 1) provide a model that is useful for circuit design; 2) use a few simple measurements as a basis for extrapolating behavior to other configurations and frequencies; and 3) provide some insight to the physical mechanisms at work. In this case, the structure being modeled is a package. The term package is used since the flipped chip creates its own package. This is clearly visible if, for example, ground bumps were placed all around the perimeter of Fig. 1. The circuits would then be enclosed by conducting planes above and below and by bump walls around the sides. Such a visualization suggests that coupling problems that occur in conventional packages can also occur in flipped chips—resonances for example. As we shall see, resonances have an important effect on isolation. This is somewhat surprising since the circuit sizes we are considering are small relative to a wavelength. However, if we take a typical chip size to be 2 mm $\times$ 2 mm and surround the perimeter with a conducting wall, the first resonance will be at 106 GHz if we discount the materials being enclosed. The resonance will be lower when the layered dielectrics are included ($\approx$65 GHz), and lower still if the wall is replaced by grounding bumps with self and mutual inductances. Many conventional isolation problems occur due to coupling between the circuit and the modes of the package even at frequencies much lower than actual resonances. Coupling to these modes is especially likely to occur at the input and output feeds of the package. This is the assumption made in the choice of topology for the model we next describe.

A. Model Topology

Fig. 2 shows the circuit topology chosen for modeling the structures in Fig. 1. The two-port labeled "MMIC" contains the circuit model or S-parameter data for the MMIC as it would be if it were deembedded from the packaging. The characteristics of this block depend entirely on the lumped, distributed, or active circuit elements on the surface of the MMIC. The two-port labeled "flipped ground plane" is the circuit-independent part of the structure and is excited at the input–output bump transitions. It controls the coupling between the input–output sides of the cavity formed by the flipped chip.

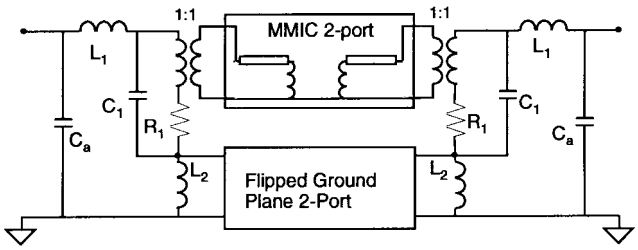

Fig. 2. Topology for a two-path circuit model of flip-mounted MMIC. The example MMIC consists of two short-circuit stubs.

The zeroth-order concept here is that current originating on the motherboard microstrip feed passes through a signal bump on to the strip conductor of, for example, a flipped microstrip. Our model assumes that the return current for this microstrip flows as image current primarily on the chip ground plane back to a point near the injecting bump. At that point the current returns to the motherboard ground mostly through the two bump grounds adjacent to the signal bump. However, the inductance of the grounding bumps causes some of the return current to flow through the other nonadjacent ground bumps, including those adjacent to the output signal bump. This causes a potential in the output loop and degrades isolation. Thus, in a sense, the currents on the elevated ground plane are split into two types, one set which is image currents to the circuitry on the chip and another set that is totally associated with the ground-bump distribution and the package structure. The ideal transformers in Fig. 2 separate these currents in the model. The inductances L_1 and L_2 are associated with the inductance of the bump transition, but L_2 controls how much the transition excites the package structure. C_1 is the capacitance between the motherboard microstrip feed line and the flip-chip ground plane in the region where they overlap. C_a is the capacitance between the microstrip and the motherboard ground plane. We take the reference planes for the microstrip feed lines to be the vertical planes abutting the ends of the flipped chip. The reference planes on the chip are located a short distance interior to the transitions (see Appendix). The resistance R_1 represents the resistive loss in the transition. The flipped coplanar and flipped microstrip both have the same circuit topology, but different component values.

The parameters of the two-port labeled *flipped ground plane* are obtained from simulating a structure derived from Fig. 1 by removing the chip circuitry, the transition bumps (including the two adjacent grounds), placing reference planes at each transition, and feeding the structure with striplines having the same cross section as the flipped chip/motherboard. Fig. 3 shows only the structure for the flipped coplanar ground-plane simulation; however, the structure for a flipped microstrip ground plane is analogous. A change in the circuitry on the surface of the MMIC will change the parameters of the two-port labeled MMIC in Fig. 2, but has no effect on the parameters of the flipped ground-plane two-port or on the lumped elements associated with the transition. The flipped ground-plane two-port parameters are affected by changing the number and distribution of the grounding bumps (excluding the transition grounds).

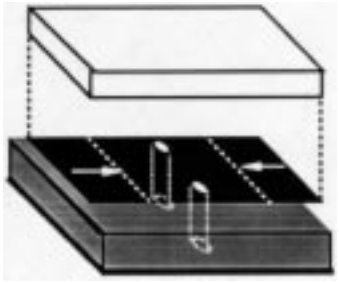

Fig. 3. Illustration of the two-port that was simulated to determine the ground-plane path characteristics of a six-bump flipped coplanar chip. Input–output transitions are eliminated leaving only the two ground bumps shown. Chip dielectric is elevated for clarity.

The transition-model component values can be evaluated using measurements or simulations of two flipped test circuits at a few low frequencies. One test circuit consists of short-circuit stubs on the MMIC, as shown in Fig. 1. The second test circuit consists of similarly placed open-circuited stubs. The impedances presented by these circuits to the on-chip reference planes are presumed to be known either from simulation or measurement. The test chips have only four bump grounds, all adjacent to the input and output signal bumps. Measurements or simulations of the mounted two-port flipped chips are taken with respect to the motherboard reference planes at low frequencies (to be specified later). In order to properly evaluate the effect of the chip substrate edge on the bump transition, a three-dimensional (3-D) simulator must be used. We used Hewlett-Packard's finite-element package HFSS[1] to simulate the test circuits. The much faster Sonnet method-of-moments package **em**[2] was used to determine the characteristics of the two-port boxes labeled "MMIC" and "ground plane" in Fig. 2.

At low frequencies, the network in Fig. 2 can be modeled entirely by lumped elements. Each short-circuit test stub can be approximated by an inductance L_t. Since in these evaluation cases there are only four grounding bumps total, the structure for the ground-plane two-port will have no grounding bumps associated with it. Thus, it looks like a short section of a microstrip transmission line, which at low frequencies can be modeled by a single-series inductance L_g, connecting between the port terminals. L_g can be found from the characteristics of any microstrip line with the same width-to-height ratio by taking the product of the microstrip impedance, phase velocity, and the length of the strip. At low frequencies the capacitive susceptances in Fig. 2 are all negligible relative to the inductive susceptances, and as a result we can simply write

$$(Z_{11}+Z_{21})_{\text{short}} \approx R_1 + j\omega(L_1+L_t+L_2) \tag{1a}$$

$$\text{Im}(Z_{21})_{\text{short}} \approx \frac{\omega L_2^2}{2L_2+L_g}. \tag{1b}$$

The left-hand side of these equations are determined from a simulation (or measurement) of the S-parameters of the entire flipped-chip short-circuit test structure followed by a conversion to Z-parameters. Since L_g is known, (1b) can be used to find L_2. L_2, in turn, can be used with the imaginary part of (1a) and the known L_t to find L_1. R_1 can be found from the real part of (1a). The sample frequencies used to evaluate these components should be small enough that the z-parameters behave inductively, but not so small that they cannot be computed or measured accurately. We simulated the structures at 1 GHz and at a couple of higher frequencies as a check.

[1]HFSS is a trademark of Hewlett-Packard, Santa Rosa, CA.

[2]**em** is a trademark of SONNET Inc., Liverpool, NY.

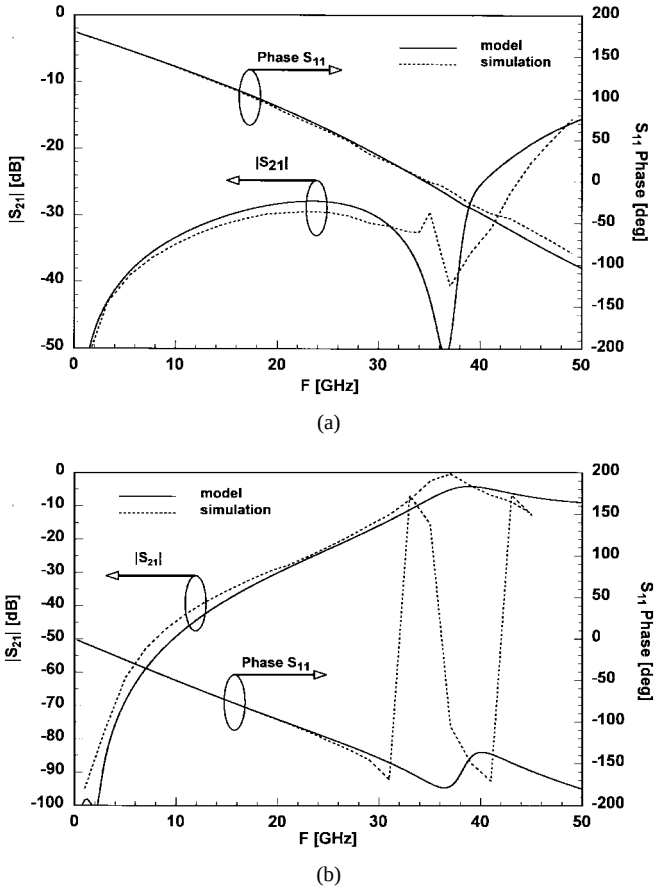

Fig. 4. Circuit model versus HFSS simulation of $|S_{21}|$ and $<S_{11}$ for a flipped coplanar chip with four bump grounds. (a) Open-circuit terminations. (b) Short-circuit terminations.

The second evaluation test circuit consists of open-circuit stubs rather than short-circuit stubs. As in the previous test, the characteristics of these stubs are determined from a separate simulation. At low frequencies, they can be modeled by shunt capacitances C_t. The ground-plane two-port is modeled as before by the series inductance L_g. From the low-frequency circuit model, the y-parameters of the flipped test circuit as seen from the motherboard reference yield the following equations:

$$\text{Im}(Y_{11})_{\text{open}} \approx \omega(C_1+C_a+C_t) \tag{2a}$$

$$\text{Im}(Y_{21})_{\text{open}} \approx \omega^2(C_1+C_t)^2\text{Im}(Z_{21})_{\text{short}} \tag{2b}$$

where $\text{Im}(Z_{21})_{\text{short}}$ was determined earlier.

The S-parameters of the flipped evaluation circuit are determined from simulation and converted to Y-parameters. The imaginary part of Y_{11} is used with C_t in (2a) to find the sum (C_a+C_1). Ideally, (2b) would then be used to find C_1. Unfortunately, Y_{21} is too small to be accurately determined at

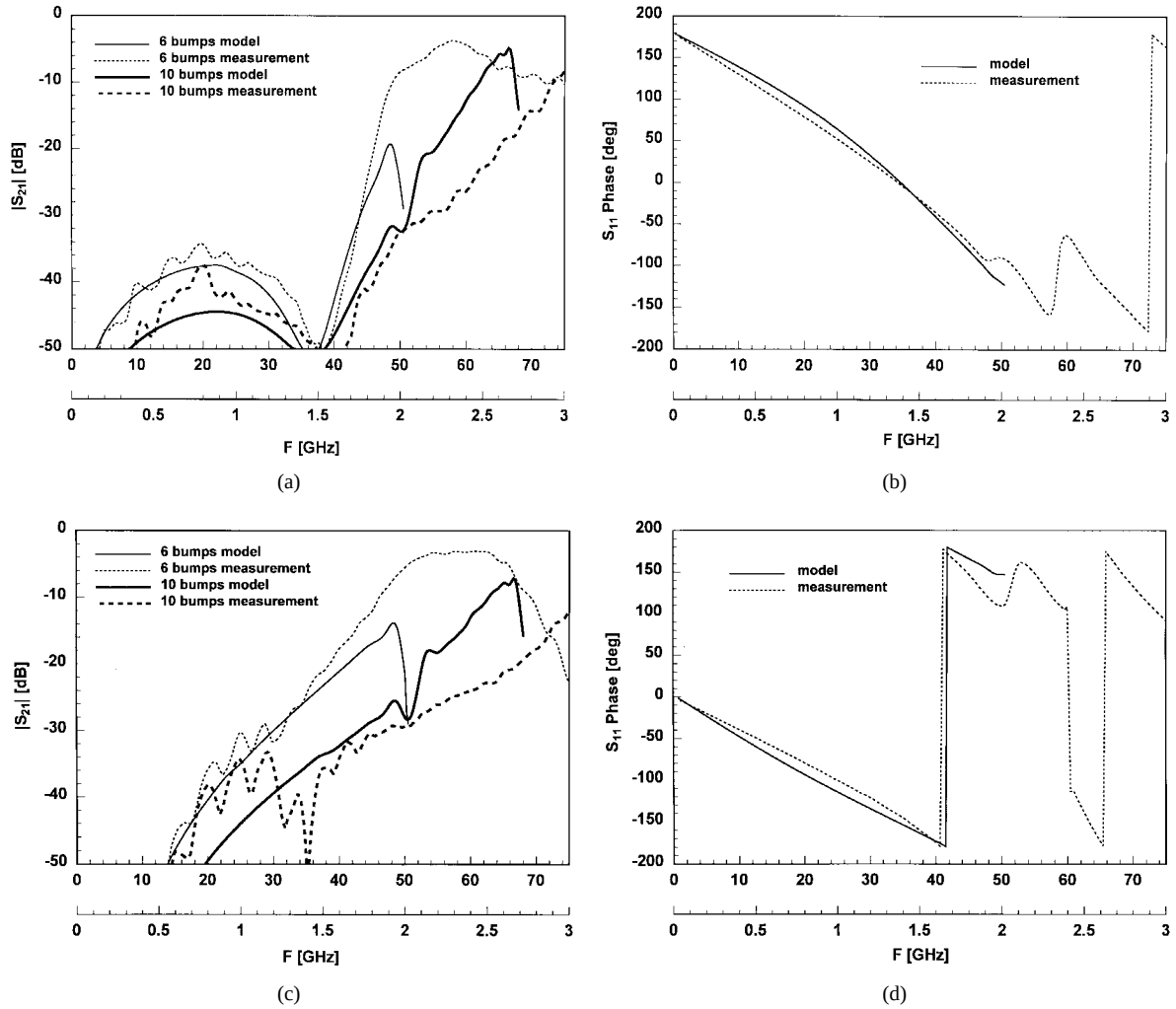

Fig. 5. Circuit model versus measurements of a scale-model coplanar flipped chip. (a) $|S_{21}|$ with short-circuit terminations, six, and ten bump grounds. (b) $<S_{11}$ with short-circuit terminations and six ground bumps. (c) $|S_{21}|$ with open-circuit terminations, six, and ten ground bumps. (d) $<S_{11}$ with open-circuit terminations and six bump grounds.

frequencies low enough for (2b) to be valid. Instead, we adjust C_1 and C_a to best fit the circuit model S_{21} to the simulated S_{21}, while keeping the quantity $(C_a + C_1)$ constant.

Once the model components are obtained, they can be applied to any MMIC circuit that would be packaged with the same bump transitions (bump height, diameter, pitch, indent from ground plane edge, etc.). Adding bump grounds beyond the two adjacent to each signal bump will change the characteristics of the flipped ground-plane two-port, but not the transition components L_1, L_2, C_1, C_a, R_1. In applying the circuit model, a data file from an **em** simulation (corresponding to Fig. 3) was used for the flipped ground two-port. However, it is likely that this could be replaced by a simple circuit model. The characteristics of the MMIC two-port were also determined from a full-wave analysis.

B. Comparison to Numerical Simulation

This modeling scheme has been applied to sample open- and short-circuit flipped chips with dimensions of 1.8 mm by 2.0 mm by 100 μm, bump heights of 50 μm, and a motherboard substrate 200 μm thick. The dielectric constants of the chip and motherboard are 10.2 (similar to GaAs) and 4.5, respectively, in order to be consistent with the experimental model to be described in the following section. The details of the test structures are supplied in the Appendix. The short- and open-terminated flip-mounted test structures were simulated on HFSS over a wide range of frequencies, and the results compared to those obtained from the circuit model. The circuit model was determined in the manner described above using HFSS. The model values are $L_1 = 0.055$ nH, $L_2 = 0.049$ nH, $C_1 = 0.085$ pF, $C_a = 0.011$ pF. Fig. 4 shows the magnitude of S_{21} and the phase of S_{11} for flipped coplanar test circuits having only four bump grounds. The agreement with the circuit model is reasonable up to 35 GHz. The phase of S_{21} has not been presented, but the agreement between numerical simulation and circuit model is similar. The magnitude of S_{11} has also not been presented since it is near unity up to 25 GHz.

Flipped microstrip circuits were also circuit modeled based on simulations of the four-bump ground test circuits at 1 GHz. The model values are $L_1 = 0.082$ nH, $L_2 = 0.080$ nH, $C_1 = 0.077$ pF, $C_a = 0.021$ pF. As in the coplanar case, S_{11} and S_{21} from the model were compared to a full wide-band simulation. The agreement was similar to the coplanar case.

III. Measurements of Scale Models

We built scale models of flipped microstrip and coplanar test chips having open- and short-circuit stubs on each port. Our goal was to measure the isolation over frequency for various numbers of ground bumps. The circuits are described in Section II and the Appendix. Our scale models are 25 times larger than these and were built using Duroid substrates having appropriate thicknesses. Brass screws and posts were used as bumps. Our measured results should approximate the actual size behavior as long as conductor loss is not an important factor. We have made measurements of models with 4, 6, 10, and 14 grounding bumps, but only the 6 and 10 bump results are presented here.

Fig. 5(a) and (c) show $|S_{21}|$ versus frequency for flipped coplanar two-ports with on-chip short- and open-circuit terminations. The upper measured frequency shown is 3.0 GHz, corresponding to 75 GHz in the unscaled chip. Each set of curves has a peak transmission, which corresponds to a resonance in the flipped chip. Adding more ground bumps moves the resonance to a higher frequency. Increasing the number of grounding bumps from 10 to 14 (not shown) moves the coplanar resonance from 75 to 85 GHz. Note that the frequency of resonance influences the isolation at much lower frequencies [see Fig. 5(c)].

Fig. 6(a) and (b) show the measured $|S_{21}|$ for flipped microstrip short- and open-circuit stub terminations. Note that the resonance frequencies are lower than in the coplanar case.

The circuit models for these structures were determined in the manner described in Section II based on HFSS simulations of the four ground-bump case at 1 GHz. One set of L_1, L_2, C_1, C_a, R_1 were determined for coplanar flipped chips and one set for microstrip. These remained unchanged for the simulations of six and ten ground bumps in Figs. 5 and 6. The only thing that was resimulated was the flipped ground-plane structure where the structure in Fig. 3 was used for the six bump ground simulation and four more ground bumps were added for the ten bump ground simulation.

Circuit model results are plotted in Figs. 5 and 6 for comparison. For short-circuit stub terminations, the measured magnitude of S_{21} agrees with the circuit model up to 35 GHz for the coplanar chips and 25 GHz for the microstrip. Similar agreement occurs for the open-circuit stub test circuits with six bump grounds. The ten bump ground measurements show qualitative agreement with the circuit model, but the measurements were somewhat sensitive at low frequency. Fig. 5(b) and (d) compare measured and modeled phase of S_{11} when six bumps ground the coplanar chip. Agreement within 15° is evident up to 30 GHz.

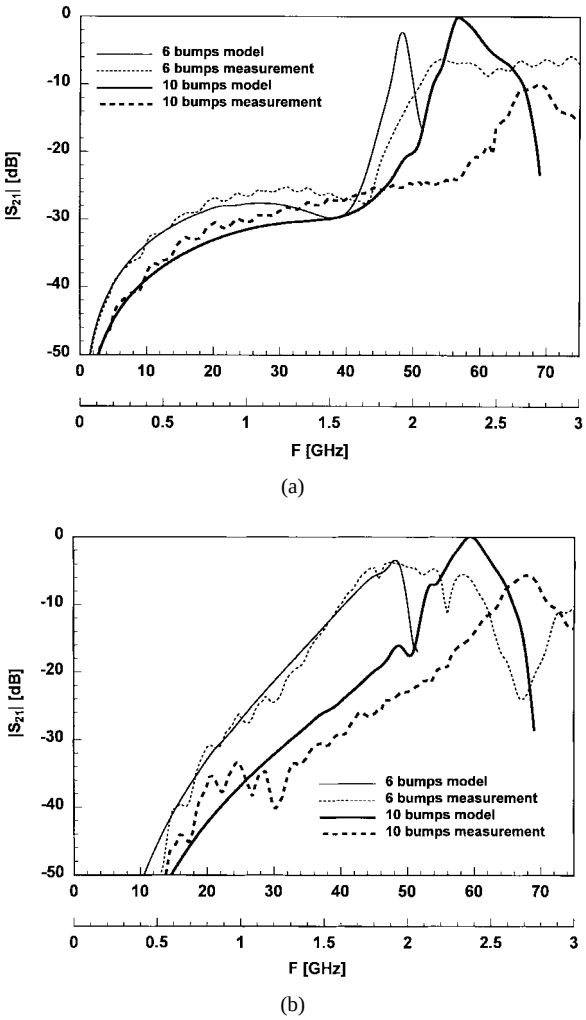

Fig. 6. Circuit model versus measurements of a scale-model microstrip flipped chip. (a) $|S_{21}|$ for short-circuit teminations with six and ten bump grounds. (b) $|S_{21}|$ for open-circuit terminations with six and ten bump grounds.

IV. Discussion

There are a number of conclusions to be drawn from the results presented above.

By comparing the worst isolation (short or open) of the coplanar chip shown in Fig. 5(a) and (c) to the worst isolation of the microstrip chip shown in Fig. 6(a) and (b), we see that the flipped microstrip has 5–10 dB less isolation than the coplanar. At frequencies above X-band, isolation appears to be correlated with the resonance frequency, which is higher for the coplanar chip than for the microstrip. The lower resonance frequency for the microstrip chip may be due to the fact that the effective permittivity beneath the flipped ground is larger due to the presence of the high permittivity chip substrate between the flipped ground plane and the motherboard ground plane.

Other simulations, not presented above show that the height of the grounding bumps makes little difference to the isolation or resonance frequency. However, the size of the chip does make a difference with smaller chips resonating at higher frequencies. As expected, Figs. 5 and 6 show that increasing numbers of bump grounds increases the resonance frequency and improves isolation.

The model we have presented in Fig. 2 shows two paths which energy can propagate from input to output, one related to the circuitry on the active face of the flipped chip and one that is related to the transition and grounding structure of the flipped ground plane. In the circuit results shown in Figs. 5 and 6, the two-port parameters for the MMIC block were obtained by **em** simulation of the unflipped and unbumped

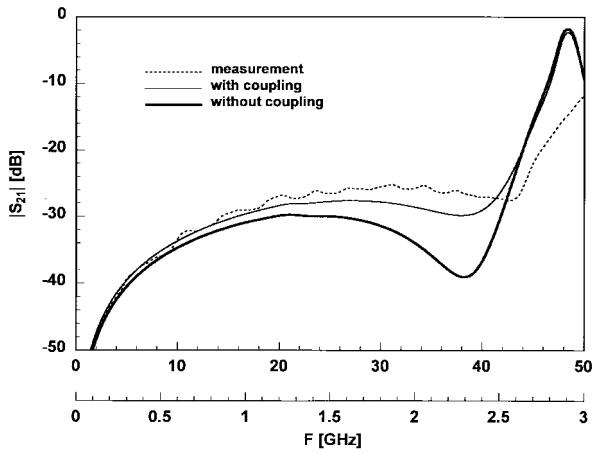

Fig. 7. Comparison of measurement to circuit model with and without internal coupling included for a flipped microstrip circuit with short-circuit terminations.

chip between the on-chip reference planes. Thus, the small on-chip coupling between the short and open circuits has been included. It is interesting to determine how important on-chip coupling is relative to the coupling through the flipped ground-plane path. Fig. 7 re-plots $|S_{21}|$ for short-circuit microstrip stubs [see Fig. 6(b)] with six ground bumps. A third curve has been added, showing the circuit modeled results when the on-chip S_{21} has been set to zero. Therefore, only the input–output transmission through the flipped ground-plane path has been included. The difference between the two curves increases with frequency. At approximately 30 GHz, the new curve is on the order of 5 dB less than the curve corresponding to the total transmission. From this, we conclude that in the case of short-circuited microstrip stubs, the on-chip coupling path is a substantial, but not dominant, transmission path from input to output. When we apply this same test to the six ground-bump microstrip open-circuited stubs, we find that the on-chip path is inconsequential relative to the ground-plane path. The on-chip coupling was also negligible for flipped coplanar open- and short-circuit stub terminations.

The circuit model topology we have chosen assumes that return currents for the traces on the MMIC surface flow entirely on the ground plane of the flipped chip, and not on the motherboard ground plane. Apparently this is a valid assumption for the cases we have studied. However, if the motherboard ground plane were closer to the circuit, this assumption may not be valid. For example, if a microstrip circuit with open-circuit terminations were flipped on to a motherboard with a ground plane on its top surface (coplanar feed), the strip trace could be closer to the motherboard ground than to the flipped-chip ground (assuming 50-μm bump height). In such a case, capacitive coupling may cause a significant return current in the motherboard ground and invalidate the proposed model. For coplanar circuits this is less likely to occur since the on-chip ground return currents are usually much closer to the signal trace than to the motherboard ground.

Lastly, because of the way we simulate the flipped ground-plane transmission, the aforementioned modeling technique has so far only been applied to feeds which are on the opposite edges of the flipped chip. We are currently working to extend the model to configurations where transitions are on adjacent sides of the flipped chip.

V. Conclusion

We have developed a two-path circuit model topology that can be used to model flipped-chip coplanar and microstrip circuits. The modeling scheme especially includes input–output isolation effects due to transitions from a microstrip motherboard. The transition model is made up of frequency-independent lumped elements, most of which can be directly extracted from low-frequency microwave measurements and/or full-wave simulations of simple test structures. Measurements of scale-model test circuits have verified the circuit model up to the lower millimeter-wave range.

The results show the existence of chip resonances occurring in the millimeter-wave range. Isolation deteriorates rapidly for frequencies approaching resonance. The chip resonance frequency can be increased by adding bump grounds or reducing chip size, both of which reduce the chip surface available for active circuitry.

Appendix

The test circuits used in this paper have the following characteristics.

A. General Characteristics

Chip size	2 mm $\times$ 1.8 mm $\times$ 0.1 mm
Motherboard thickness	0.2 mm
Chip dielectric constant	10.2
Motherboard dielectric constant	4.5
Bump height	50 μm
Motherboard via diameter	100 μm
Bump cross section	100 μm
Microstrip feedline Z_o	50 Ω
Bump pitch at transition	151 μm
Motherboard reference planes	beneath chip edges
Bump indent from edge	225 and 90 μm

B. Coplanar Test Circuits

CPW strip width/cross section	40/120 μm
Metallization gap surrounding input–output bump	25-μm, interior: 50-μm, exterior: 30-μm, sides
Length of short-circuit stub from bump center	425 μm
Length of open-circuit stub from bump center	425 μm to end gap 50 μm
Chip reference plane	75 μm from bump center

C. Microstrip Test Circuits

Strip width	73.7 μm
Length of open-circuit stub from bump center	425 μm

Length of short-circuit stub from bump center to via center	475 μm
Via cross section	100-μm square
Chip reference plane	112.5 μm from bump center

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